

AMENDMENTS TO THE CLAIMS

Claim 1 (Original): A wireless communication system for hosting a plurality of processes, each process in said plurality of processes executed in accordance with a communication protocol, the communication protocol including a set of functions, said wireless communication system comprising:

a plurality of application specific instruction set processors (ASISPs), each ASISP capable of executing a subset of said set of functions included in said communication protocol; and

a scheduler connected to said plurality of ASISPs for scheduling said plurality of ASISPs in accordance with a time-slicing algorithm so that each process in said plurality of processes is supported by said wireless communication system.

Claim 2 (Original): The wireless communication system of claim 1 wherein each said ASISP in said plurality of ASISPs further comprises:

an input register for receiving an input program and state associated with a process in said plurality of processes, each instruction in said input program being part of a limited purpose instruction set that supports said subset of functions included in said communication protocol; and

an output register for storing a value that indicates a state of said process after execution of said input program.

Claim 3 (Original): The wireless communication system of claim 2, wherein

said input program is associated with a first process selected from said plurality of processes; and

said time-slicing algorithm includes a step of allocating a selected ASISP in said plurality of ASISPs to said input program for a predetermined period of time.

Claim 4 (Original): The wireless communication system of claim 3 wherein said input program is not interrupted by said scheduler during said predetermined period of time.

Claim 5 (Original): The wireless communication system of claim 3 wherein execution of said input program is completed during said predetermined period of time.

Claim 6 (Original): The wireless communication system of claim 2, wherein said scheduler further includes a synchronization mechanism for synchronizing said plurality of ASISPs, the synchronization mechanism capable of reallocating an ASISP in said plurality of ASISPs from a first input program that is associated with a first process to a second input program that is associated with a second process.

Claim 16 (Original): The wireless communication system of claim 15 wherein said communication protocol is IS-136 TDMA.

Claim 17 (Original): The wireless communication system of claim 1 wherein said ASISP is a finger ASISP and said subset of functions comprises a delay lock loop (DLL) and a channel estimation.

Claim 18 (Original): The wireless communication system of claim 1 wherein said ASISP is a combiner ASISP and said subset of functions comprises a frequency error estimation, a finger energy estimation, and a signal-to-interference (SIR) estimation.

Claim 19 (Original): The wireless communication system of claim 1 wherein each process in said plurality of processes is an echo.

Claim 20 (Original): The wireless communication system of claim 1 wherein each process in said plurality of processes uniquely corresponds to a different mobile hosted by said wireless

communication system and each said process combines a plurality of echoes associated with the corresponding different mobile.

Claim 21 (Original): The wireless communication system of claim 1 wherein each said ASISP in said plurality of ASISPs is capable of executing said subset of said set of functions on a time-scale of about 400 to about 5,000 times per second.

Claim 22 (Original): The wireless communication system of claim 1 wherein each said ASISP in said plurality of ASISPs further comprises:

an input register for receiving an input program associated with a process in said plurality of processes, each instruction in said input program being part of a limited purpose instruction set that supports said subset of functions included in said communication protocol; and

each instruction in said limited purposed instruction set includes an arithmetic logic unit field, a load field, and a load/store field.

Claim 23 (Original): A method for reducing an amount of inter-process overhead between computing components in a device capable of hosting a plurality of communication processes, each communication process in said plurality of communication processes operating in accordance with a communication protocol, comprising:

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distributing a plurality of application specific instruction set processors (ASISPs), each ASISP capable of executing a subset of a set of functions in accordance with said communication protocol; and

providing a centralized controller for sending control commands to each said ASISP in said plurality of ASISPs; wherein

said centralized controller schedules the functions calculated by each said ASISP in said plurality of ASISPs in a master/slave relationship, thereby reducing said amount of inter-process overhead between said computing components in said device.

Claim 24 (Original): A method for hosting a communication process with a communication architecture in accordance with a communication protocol, comprising:

allocating a plurality of application specific instruction set processors (ASISPs) in said architecture to support said communication process, each ASISP in said plurality of ASISPs capable of executing a subset of a set of functions defined by said communication protocol; and

providing a centralized controller in said architecture for scheduling each said ASISP in said plurality of ASISPs in accordance with a scheduling scheme.

Claim 25 (Original): The method of claim 24, wherein each said ASISP in said plurality of ASISPs is dimensioned and configured for receiving scheduling commands and process state information

from said centralized controller, wherein said process state information describes a state of said communication process.

Claim 26 (Original): The method of claim 25, wherein each said ASISP in said plurality of ASISPs receives input from non-scheduling control blocks in said communication architecture in addition to said scheduling commands from said centralized controller.

Claim 27 (Original): The method of claim 24, wherein said scheduling scheme is a time-slicing algorithm that allocates computational tasks to each ASISP in said plurality of ASISPs in a time-sliced fashion.

Claim 28 (Original): The method of claim 24 wherein a first group of ASISPs in said plurality of ASISPs are dimensioned and configured to perform finger calculations and a second group of ASISPs in said plurality of ASISPs are dimensioned and configured to perform combiner calculations.

Claim 29 (Original): The method of claim 28 wherein said subset of functions associated with each ASISP in said first group of ASISPs comprise a delay lock loop (DLL) and a channel estimation.

Claim 30 (Original): The method of claim 28 wherein said subset of functions associated with each ASISP in said second group of ASISPs comprise a frequency error estimation, a finger energy estimation, and a signal-to-interference (SIR) estimation.

Claim 31 (Original): A method for hosting a plurality of processes in a wireless communication system, each process in said plurality of processes executed in accordance with a communication protocol, the communication protocol including a set of functions, comprising:

distributing a plurality of application specific instruction set processors (ASISPs), each ASISP capable of executing a subset of said set of functions included in said communication protocol; and

providing a scheduler for scheduling said plurality of ASISPs in accordance with a time-slicing algorithm so that each process in said plurality of processes is supported by said wireless communication system.

Claim 32 (Original): The method of claim 31 wherein each said ASISP in said plurality of ASISPs is dimensioned and configured to provide:

an input register for receiving an input program and state associated with a process in said plurality of processes, each instruction in said input program being part of a limited purpose instruction set that supports said subset of functions included in said communication protocol; and

an output register for storing a value that indicates a state of said process after execution of said input program.

Claim 33 (Original): The method of claim 32, wherein

said input program is associated with a first process selected from said plurality of processes; and

said time-slicing algorithm includes a step of allocating a selected ASISP in said plurality of ASISPs to said input program for a predetermined period of time.

Claim 34 (Original): The method of claim 33 wherein execution of said input program is completed during said predetermined period of time.

Claim 35 (Original): The method of claim 32, wherein said scheduler further includes a synchronization mechanism for synchronizing said plurality of ASISPs, the synchronization mechanism capable of reallocating an ASISP in said plurality of ASISPs from a first input program

that is associated-with -a-first process to a second input program that is associated with a second process.

Claim 36 (Original): The method of claim 35 wherein said first process is a first echo and said second process is a second echo.

Claim 37 (Original): The method of claim 35 wherein said first process is each echo associated with a first mobile and said second process is each echo associated with a second mobile.

Claim 38 (Original): The method of claim 32, wherein

said time-slicing algorithm defines a predetermined period of time;

said limited purpose instruction set includes a "wait" instruction for synchronization; and

each ASISP in said plurality of ASISPs is configured so that when said "wait" instruction is received by said input register, the ASISP does execute a communication protocol function during said predetermined period of time and then automatically returns to an idle state thereby reducing a power consumption of the ASISP during the predetermined period of time.

Claim 39 (Original): The method of claim 32, further comprising

distributing a plurality of memory modules, each memory module in said plurality of memory modules associated with a different ASISP selected from said plurality of ASISPs.

Claim 40 (Original): The wireless communication system of claim 39 wherein said state of said process stored in said output register is stored in a unique segment of said different memory module, the unique segment of said memory module being determined by an identity of said process.

Claim 41 (Original): The method of claim 40 wherein said output register is further used to store a process identifier value that provides said identity of said process.

Claim 42 (Original): The method of claim 31 wherein said communication protocol is a code division multiple access (CDMA) protocol.

Claim 43 (Original): The method of claim 42 wherein said communication protocol is selected from the group consisting of IS-95 CDMA, IS-95B CDMA, CDMA TIA IS2000, TIA IS 2000A, wideband CDMA (WCDMA), cdma2000, and ARIB WCDMA.

Claim ~~42-44~~ (Presently Amended): The method of claim 31 wherein each process in said plurality of processes is an echo.

Claim ~~43-45~~ (Presently Amended): The method of claim 31 wherein each process in said plurality of processes uniquely corresponds to a different mobile hosted by said wireless communication system and each said process combines a plurality of echoes associated with the corresponding different mobile.

Claim ~~44-46~~ (Presently Amended): The method of claim 31 wherein each said ASISP in said plurality of ASISPs is capable of executing said subset of said set of functions on a time-scale of about 400 to about 5,000 times per second.

Claim ~~45-47~~ (Presently Amended): The method of claim 31 wherein each said ASISP in said plurality of ASISPs further comprises:

an input register for receiving an input program associated with a process in said plurality of processes, each instruction in said input program being part of a limited purpose instruction set that supports said subset of functions included in said communication protocol; and

each instruction in said limited purposed instruction set includes an arithmetic logic unit field, a load field, and a load/store field.